Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A packet switched communications system for transmitting synchronous data from a source module to a terminating module over a network, the network comprising plurality of modules interconnected via transmission links, each module ~~operating within~~in the network having a clock of nominal frequency ~~but which~~ that is not ~~synchronised~~ synchronized with the clocks of the other module(s) in the network and having a single input and one or more outputs where all the outputs of each module are phase locked to each other but are not ~~synchronised~~ synchronized with respect to the input, means for determining [[the]] an accumulated phase difference between [[the]] an input clock and [[the]] an output clock of each module, means for transmitting the accumulated phase difference to the terminating module~~ in the network~~, and means for ~~utilising~~ utilizing the received accumulated phase difference at the terminating module to lock [[the]] an output clock at the terminating module to [[the]] an input clock at the source module.

2. (Original) A system as claimed in Claim 1 in which the accumulated phase difference is transmitted at regular intervals in an ATM data cell.

3. (Previously presented) A system as claimed in Claim 1 in which the determining means comprises a first counter for counting clock cycles of the input signal clock, a second counter for counting cycles of the output signal clock, and means for simultaneously reading the counts of the first and second counters.

4. (Original) A system as claimed in Claim 3 comprising a latch for storing the count of the counter counting the higher frequency clock, the count being clocked into the latch by an edge of the lower frequency clock.

5. (Previously presented) A system as claimed in Claim 3 in which the means for transmitting the phase difference comprises means for assembling an ATM cell containing the counts of the first and second counters.

6. (Currently amended) A method of recovering clock signals in a packet switched communications network, the network comprising a plurality of modules interconnected via transmission links, each module ~~operating with~~ having a clock of nominal frequency ~~but which~~ that is not ~~synchronised~~ synchronized with the clocks of the other module(s), [[and]] each module having a single input and one or more outputs, wherein all the outputs of each module are phase locked to each other but are not ~~synchronised~~ synchronized with ~~respect to~~ the input, the method comprising the steps of:

a) determining the accumulated phase difference between [[the]] an input clock and [[the]] an output clock at each module,

b) transmitting the determined accumulated phase difference to [[the]] a terminating module, and

c) ~~utilising~~ utilizing the received accumulated phase difference at the terminating ~~network~~ module to recover the clock at [[the]] a source module of the network.

7. (Previously presented) A method as claimed in Claim 6 in which the network uses asynchronous transfer mode (ATM) and the accumulated phase difference is transmitted in an ATM cell.

8. (Previously presented) A method as claimed in Claim 6 in which step a) comprises the steps of:

d) applying the input clock of a module to a first counter within the module,

e) applying the output clock of the module to a second counter within the module,

f) reading the counts of the first and second counters simultaneously at given intervals.

9. (Original) A method as claimed in Claim 8 in which step d) comprises transmitting the counts read in step f).

10. (Previously presented) A method as claimed in Claim 8 in which the counters are read on a transition of the lower frequency clock.

11. (Previously presented) A system as claimed in Claim 2 in which the determining means comprises a first counter for counting clock cycles of the input signal clock, a second counter for counting cycles of the output signal clock, and means for simultaneously reading the counts of the first and second counters.

12. (Previously presented) A system as claimed in Claim 11 comprising a latch for storing the count of the counter counting the higher frequency clock, the count being clocked into the latch by an edge of the lower frequency clock.

13. (Previously presented) A system as claimed in Claim 4 in which the means for transmitting the phase difference comprises means for assembling an ATM cell containing the counts of the first and second counters.

14. (Previously presented) A system as claimed in Claim 11 in which the means for transmitting the phase difference comprises means for assembling an ATM cell containing the counts of the first and second counters.

15. (Previously presented) A system as claimed in Claim 12 in which the means for transmitting the phase difference comprises means for assembling an ATM cell containing the counts of the first and second counters.

16. (Previously presented) A method as claimed in Claim 7 in which step a) comprises the steps of:

d) applying the input clock of a module to a first counter within the module,

e) applying the output clock of the module to a second counter within the module,

f) reading the counts of the first and second counters simultaneously at given intervals.

17. (Previously presented) A method as claimed in Claim 16 in which step d) comprises transmitting the counts read in step f).

18. (Previously presented) A method as claimed in Claim 9 in which the counters are read on a transition of the lower frequency clock.

19. (Previously presented) A method as claimed in Claim 16 in which the counters are read on a transition of the lower frequency clock.

20. (Previously presented) A method as claimed in Claim 17 in which the counters are read on a transition of the lower frequency clock.